



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/851,277	05/08/2001	Tae-Sung Jung	5649-894	3420
20792	7590	02/10/2005	EXAMINER	
MYERS BIGEL SIBLEY & SAJOVEC PO BOX 37428 RALEIGH, NC 27627			FLEMING, FRITZ M	
			ART UNIT	PAPER NUMBER
			2182	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/851,277

Applicant(s)

JUNG ET AL.

Examiner

Fritz M Fleming

Art Unit

2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 November 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 May 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Fritz M. Fleming
FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-3,5,11-13,15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi in view of Kaneko et al.

The indicated claims are being rejected as being obvious over Adachi in view of Kaneko et al. First, turning to claim 1, it is to be noted that this claim only require a memory interface system with the channel line coupling the memory to the memory controller with the line being responsive to a terminal voltage that is independent of the other supplies. Please note, that the claim only requires a "responsive" without further defining this facet. Hence, turning to Adachi, one finds a memory card 14 that is either powered by a 3V or 5V source, with certainly the indication that the voltage source is contained in the memory card, as there is no supply passing from the camera 1 thereto, as the only connection points are the at least one channel lines 122,124 that couple the memory 14 to the memory controller 10, such that the at least one channel lines are responsive to either the 3V or 5V source of the camera. As the 3V and 5V sources of the camera 1 are shown to be independent as they are not connected nor shown to be of a common source, they are thus as independent as applicants have shown and claimed. Thus in a situation when the memory card 14 is supplied at a 3V level, the switch 126 makes lines 122/124 and level shifter 20 and lines 114/112 responsive to the terminal voltage of the 3V camera supply, which is in turn independent of the camera's 5V supply. Note also that the rest of 16, not including level shifter 24, is also supplied by the 3V supply, thus making the terminal voltage, to which the channel lines 122/124 are responsive, independent of the 5V supply powering the memory controller 10. What is missing is evidence that memory card has its own independent supply, which would

Art Unit: 2182

thus make the supplies of the memory, the memory controller and the channel lines independent, to the extent claimed.

Thus one of ordinary skill in the art is motivated to look for cameras with memory cards, to see how these cards are supplied. One example of such is Kaneko et al., in which one finds a camera 20 with its own supply 35 and a memory card 50 with its own built in battery 51. Please refer to the English language abstract and Figure 1, which clearly show the independent supplies of the memory and the camera.

Therefore it would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify Adachi per the teachings of Kaneko et al. as Kaneko et al. have shown that it is old and well known in the art to supply a camera and its memory card via separate and independent power supplies. Thus in combination, when Adachi is operated with a memory card supplied by its own independent 3V source, as shown per Kaneko et al. to be independent, the channel lines 122/124 and the level shifter 20 and the logic circuit 22 are thus all powered by, and hence responsive to, the camera's 3V supply, which is also independent of the camera's 5V supply. Also note in Kaneko et al. that a plurality of independent supplies are shown in the camera at 35 and 37, which are also shown to be of differing voltages noting the conventional symbology for each battery. When the memory card is operable connected, the memory thus comprises the first receiver 21b and transmitter 21a in the level shifter 20, and the memory controller comprises also the second receiver 25a and transmitter 25b in the second level shifter, wherein at least one channel line 114/112 and 116/110, responsive to the 3V supply, serve to couple the first and second

Art Unit: 2182

receivers/transmitters, per claim 2. Thus per claim 3, the first receiver/transmitter is powered by the 3V supply and the second receiver/transmitter is powered by the 5V supply that supplies the controller. While the 3V supply powering the first receiver/transmitter is in the camera, it is a mere substitution of supplies to power such via the memory card battery when it is operating at 3V, thus rendering such obvious. Turning to claim 5, the level shifters serve to provide a coupling function, with 20 coupling 124 to 21a to 114 to 116 and 20 coupling 110 to 112 to 21b to 122. Note that the breadth of the coupling allows for the references to meet what is claimed. As both references process data to the extent claimed, claims 11-13 and 15 are rejected for the same reasons.

5. Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi in view of Kaneko et al. as applied to claims 1-3,5,11-13,15 above, and further in view of Taguchi.

Turning to claims 10 and 20, the combined teachings of Adachi and Kaneko et al. lack the express teaching that the terminal voltage magnitude be greater than the others. Turning to Taguchi, one finds a similar setup in which the terminal voltage of the coupling line 10 is at 2.5V, the same level as the other sources. However, it is expressly taught at column 8, lines 4-9, that to increase the terminal voltage above 2.5V results in further enhanced performance, thus increasing the coupling line voltage to a value higher than used in the devices 20, which are memories and memory controllers. Therefore it would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify Adachi and Kaneko et al. per the teachings of

Taguchi, so that the coupling lines are responsive to the highest voltage magnitude in order to further enhance performance.

6. Claims 4,6-9,14,16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi in view of Kaneko et al. as applied to claims 1-3,5,11-13,15 above, and further in view of Taguchi.

Turning to claims 4,6-9,14,16-19, one finds that Adachi in view of Kaneko et al. lack the specifics of the transmitters and receivers. Turning to Suh, one finds that it is conventional in the art of memory bus interface circuits to use a coupling bus 12 that is responsive to a terminal voltage V_{tt} , with a transmitter 11 and receiver 13, wherein the receiver uses a reference voltage, and the transmitter is independent of other voltages as it driven at its gate and not supplied by a separate source, as it too is responsive to the terminal voltage (i.e. connected the same way as applicants' 102). Per column 1, the driver/transmitter is of the open drain structure and are MOS transistors. The receivers in the form of 13 are comparators per columns 1 and 2, wherein comparators are commonly made from differential amplifiers, per column 4. Note also that each receiver has a corresponding reference voltage and is responsive to the data carried on the coupling bus line, with the same type of connections as applicants have shown in their Figure 2. Advantages of Suh include things such as decreased common mode noise, influence of ground bounce, and the like per column 2, lines 30+, which parallel applicants' Figure 2 layout. Therefore it would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the combined teachings of Adachi and Kaneko et al. per the teachings of Suh in order to include open

Art Unit: 2182

drain transmitters and comparator/differential amplifier receivers in the memory and controller, so as to decrease common mode noise, influence of ground bounce. When combined, the transmitters and receivers of Suh would be placed in the level shifters of Adachi such that the transmitters are located in the memory to input to the level shifter 21a and in the controller to input to level shifter 25b, and the receivers to receive the data at 142 from 25a and at 122 to receive the data from 21b. Hence the level shifters serve to couple the discrete receivers as claimed.

7. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suh in view of Merritt and Taguchi.

Additionally, the teachings of Suh and Merritt and Taguchi can be combined as follows, to render claims 1-20 as obvious. Suh, the primary reference, in Figures 3 and 5, shows receivers recA/B of the differential amplifier type comparator (see column 4) and MOS transistor open drain transmitter drivers (per Figure 1, also called open driver structure at column 2+) coupled via a channel line 12, wherein the channel line 12 is responsive to a terminal voltage V_{tt} . Use is in a high-speed memory interface per column 3, lines 43-47, but express mention of the memory and memory controller is lacking, noting that data is clearly sent and received from chip to chip. In Figures 3 and 5, there are two separate and distinct chips shown in outline form and these are connected by the channel line. As such, the V_{tt} comes from outside of each chip, and is thus "independent" of these chips. As a point of comparison, applicants, page 4, lines 15, states that the VTER may be supplied from an external voltage source, and the discussion of Figure 2, lines 10-15 of page 7, reveal that the supply voltages are

Art Unit: 2182

independent (i.e. all one can gather from the applicants' Figure 2 is about the same as what Suh has shown, that being an "independent" voltage supply means to be from an area outside of the dashed lines encompassing the other chips) and that per page 8, independent supplies mean that VTER can be increased above the values of VDD1 and VDD2 in order to improve signal to noise ratio. Hence, alone Suh meets one of the tests of Vtt being "independent" in that the Vtt is shown to be "off chip" when compared to the chip outlines of Figures 3 and 5, thus being shown to be the same "independent" as applicants have shown, as far as being "off chip" is concerned. However, Suh does not expressly teach the other aspect of an "independent" Vtt, that being the ability to increase Vtt above the values used in the chips, as applicants have shown

"independent" to mean an "electrical independence" per column 3, lines 12-15, and the "off chip" locations of VTERM in the Figures. Turning to Merritt, one finds that the chips have their own independent power supplies. For example, 200 qualifies as a memory controller, 100 is the memory, and there is a line coupling the two for data transmission at VIN. Per column 3, lines 59+, one finds explicit teachings that the power supplies 30 and 230 for the respective sections 100 and 200 are independent and operate at different voltage levels. Hence, Merritt, when applied to Suh, sets forth that each chip will have its own independent supply, and thus since the Vtt is supplied from outside the two chips, the 3 power supplies are independent to the extent shown in applicants' Figures. Now turning to Taguchi, the final part of power supply independence is taught. Similar to both Suh and what applicants have set forth, there are devices 30 coupled to a bus 10, which bus 10 is supplied by VTT. Note that each device 30 includes an open

Art Unit: 2182

drain driver 31 and an input buffer 33, which has also as an input, a reference voltage.

As pointed out in an earlier discussion of Taguchi, the material spanning columns 7 and 8 set forth the "voltage magnitude independence" of V_{tt} by explicitly teaching the

positive aspects of raising the level of V_{tt} above 2.5V, thus being above the power

voltage of the devices running at 2.5V (as seen in Figure 9), with advantages to include

a further enhancement in performance. Thus it would have been obvious to one having

ordinary skill in the art at the time that the invention was made to modify Suh by the

teachings of Merritt and Taguchi in order to have an independent terminal voltage which

results in further performance enhancements. Thus the limitations of claims 1,10,11,20

have been addressed, noting that the systems combined set forth a "data processing

system". For claims 2 and 12, note that Suh sets forth that each chip has its own

transmitters and receivers, with a transmitter connected to a receiver by a channel line

that is responsive to the terminal voltage V_{tt} , as seen in Figures 3 and 5 wherein $drvA1$

is coupled to $recB1$ via 12 and $drvBn$ is coupled to $recAn$ by another 12. Note also that

Suh teaches use in a memory interface and Merritt teaches a memory coupled to a

memory controller. Regarding claims 3 and 13, note that Merritt teaches that each chip

has its own independent source. Regarding claims 4 and 14, the transmitters of both

Suh and Taguchi are "independent" in so far as they are connected to the bus in the

same manner as those of applicants. Regarding claims 5 and 15, Taguchi teaches a

level shifter 51-54 at the input buffer 33, which is also in the form of a differential

amplifier. See column 8, lines 26+ and the discussion of Figure 9. Since Taguchi

teaches a level shifter at the input buffer of a device 30, then in combination, all devices

Art Unit: 2182

with input buffers (i.e. receivers) would also be equipped with a level shifter, thereby rendering obvious the first and second circuits. Regarding claims 6 and 16, the open drain transmitters are taught by Suh and Taguchi. Regarding claims 7-9 and 17-19, both Suh and Taguchi teach the use of reference voltage input receivers/buffers made up from differential amplifiers. As such, they are responsive to the data carried on these lines, as well as the reference voltages, as Suh clearly shows such a setup in Figures 3 and 5. See also the details of Taguchi's Figure 9. Again, level shifters at the input buffers are seen in Taguchi's Figure 9, thus the addition of such to Suh's receivers, which are the equivalent of the input buffers, is obvious subject matter, in order to benefit from Taguchi's level shifter (per column 8, lines 50+), expressly for better detection of the high/low status of the input signal.

Response to Arguments

1. Applicant's arguments, see amendment, filed 11/18/2004, with respect to the rejection(s) of claim(s) 1-20 under Suh, Tsern, Merritt and Adachi have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Adachi and Kaneko et al., as well as Suh and Merritt and Taguchi.


The argument provided by applicants has been persuasive to remove the grounds of rejection for the remaining claims 1-20. However, a new grounds of rejection is presented below, based upon a re-evaluation of the cited references in light of the comments provided by applicants. Accordingly, this rejection is not made final, as it was not necessitated by amendment.

Art Unit: 2182

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fritz M Fleming whose telephone number is 571-272-4145. The examiner can normally be reached on M-F, 0600-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 571-272-4146. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Fritz M Fleming
Primary Examiner
Art Unit 2182

fmf